

FPGA-based All-digital SDR System

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Abstract

Next generation 5G wireless communications will deliver gigabit per second data rates with both base-stations and mobile devices capable of operating at a vast range of frequencies. Additionally, an increasing use of new wireless standard using different frequencies, diverse coding and modulation schemes and targeting different applications is also taking place. In scenarios of this nature, a highly flexible, power efficient and wideband radio transceiver is required to be capable of adapt itself to the communication environment changes. In fact, for such approach, the physical layer of the radio must be able to support the simultaneous transmission of multi-band, multi-rate and multi-standard signals which is unpractical or inefficient with conventional radio architectures. Within this context it is emerging the possibility to build all-digital FPGA-based Software Defined Radio (SDR) transceivers, which is very attractive in terms of answering the previous requirements. This demonstration presents a FPGA-based all-digital SDR end-to-end communication system with both transmitter and receiver implemented using medium-range FPGAs.

Transceiver Architecture

- An original FPGA-based all-digital transceiver architecture
- Highly flexible architecture
- Analog-to-digital conversion based on PWM
- High analog input bandwidth up to 3 GHz
- RF digital transmitter based on Delta-Sigma modulation
- Any carrier frequency transmission up to 2.4 GHz
- Tx EVM below 1.5% up to 2.4 GHz
- Rx EVM below 4% up to 2.4 GHz

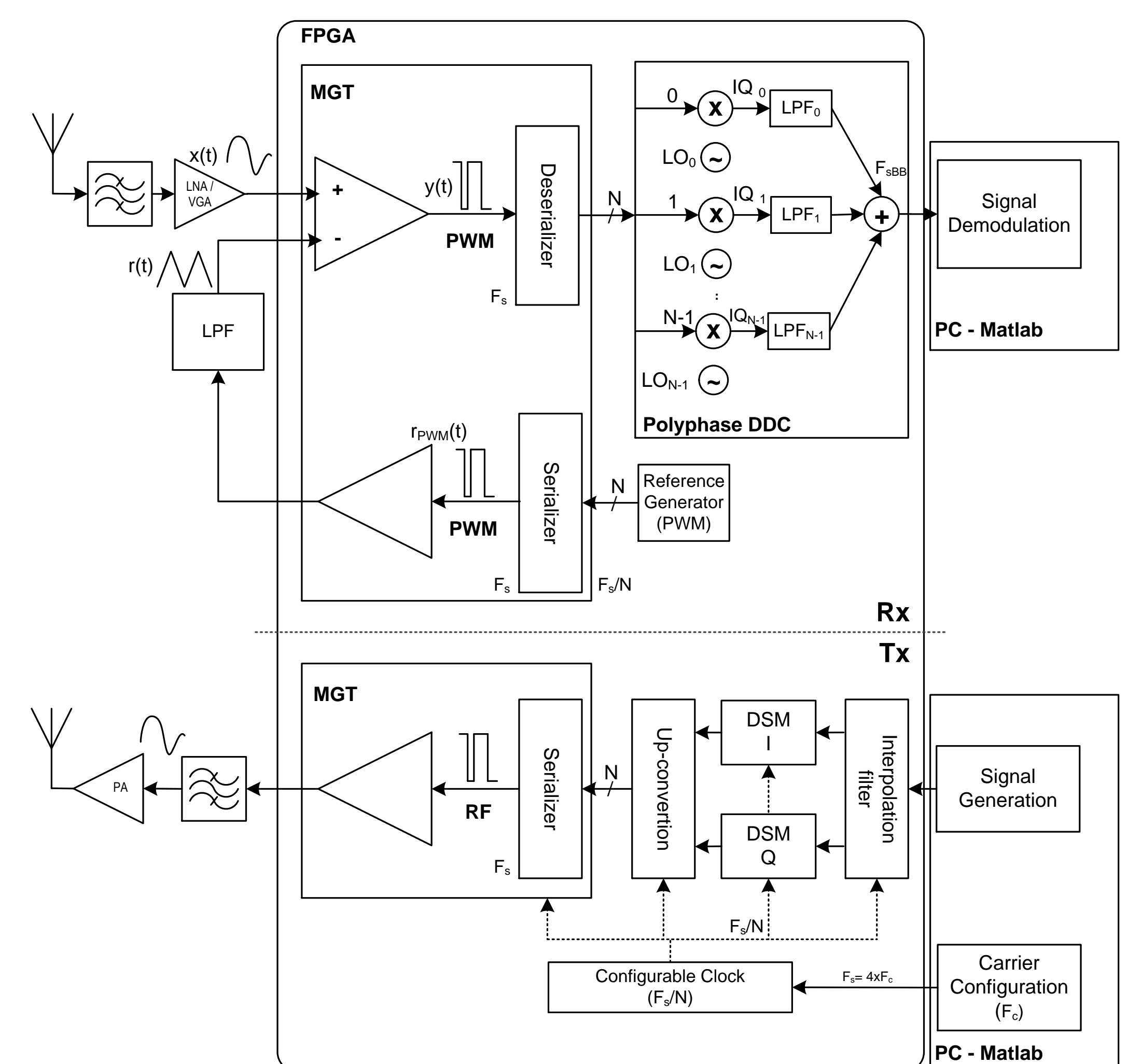


Fig. 1 - Block diagram representation of the proposed all-digital transceiver architecture.

Results

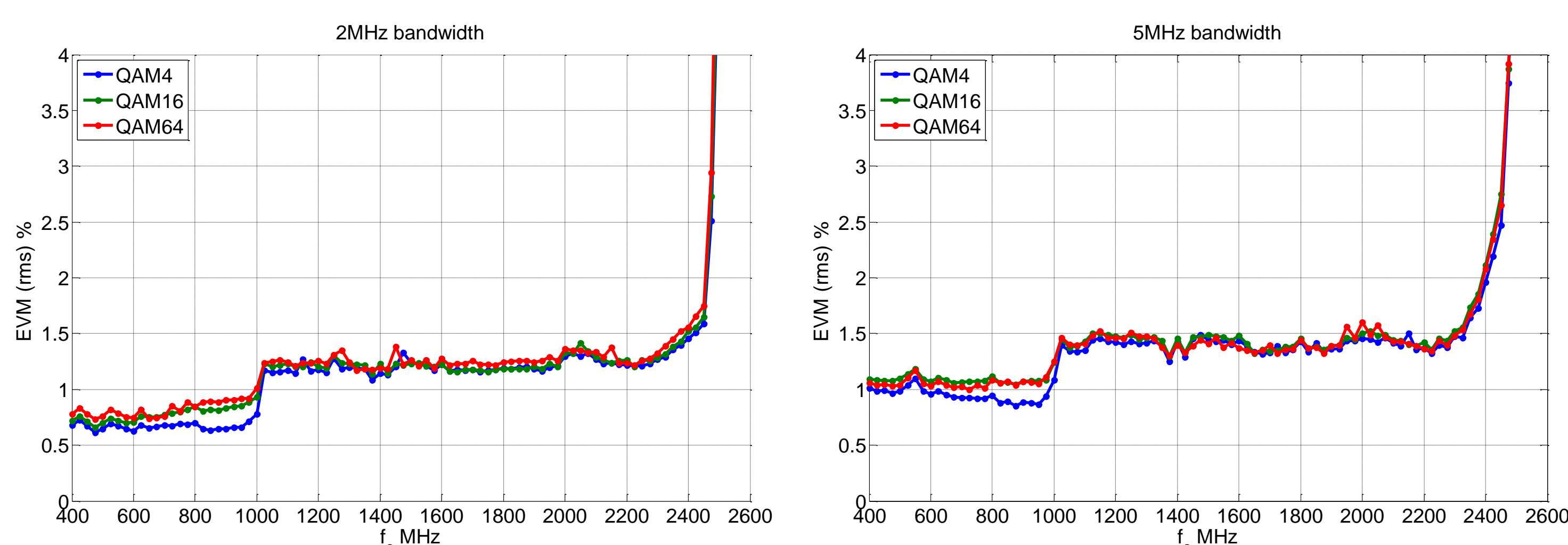


Fig. 2 - Measured transmitter EVM results over the carrier frequency using 2MHz and 5MHz signals for QPSK, 16-QAM and 64-QAM modulations.

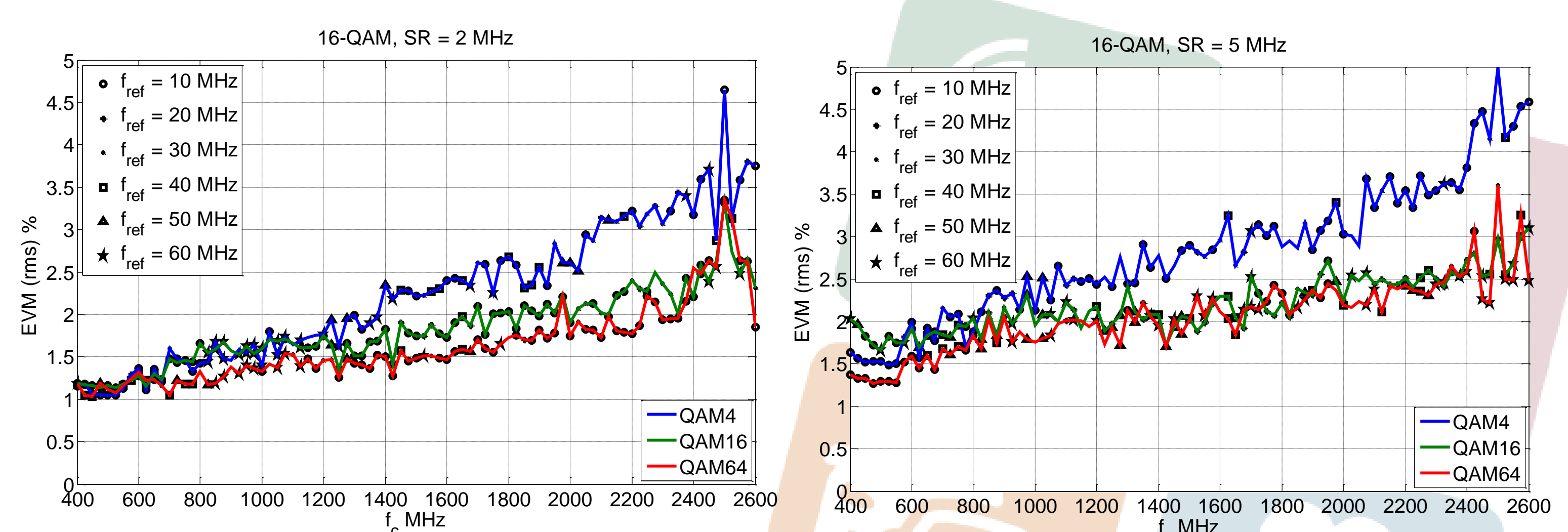


Fig. 3 - Measured and simulated results of EVM over the carrier frequency using a 2MHz and a 4MHz 16-QAM signal.