AIDA

ANALOG IC DESIGN AUTOMATION

The AIDA project addressed the problem of analog and mixed-signal (AMS) IC design automation. It introduced an innovative circuit-level synthesis methodology based on evolutionary computation techniques, which was implemented in AIDA-C and AIDA-L, in-house developed tools, respectively, for the automation of circuit sizing and optimization, and layout generation tasks. The proposed solution was validated for several analog circuit building blocks of different levels of complexity, such as, operational amplifiers, LNAs, LC-VCOs, etc. and adopted at the end by an international industrial partner.

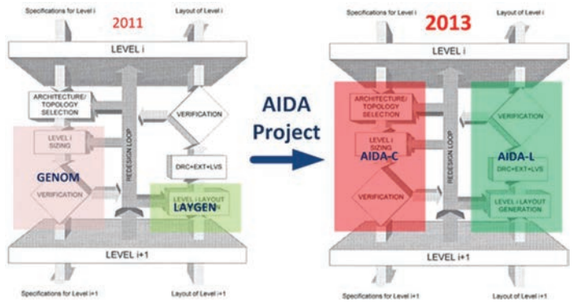

Fig.1 AIDA Project Contribution to Analog IC Design Automation.

The AIDA project addressed the analog IC design automation. First, by putting together a multidisciplinary team including experts in Computer-Aided Design (CAD), Evolutionary Computation (EC) and Analog IC Design, and also by incorporating people from different institutions and different research groups. Then, by evaluating the state-of-the-art on analog IC design automation and proposing an disruptive and innovative circuit-level synthesis methodology based on evolutionary computation techniques. Finally, by implementing the proposed methodology taking into account the previous team work, namely, GENOM and LAYGEN, in the area, resulting in the AIDA design environment, which incorporates AIDA-C, a circuit level sizing and optimization tool, and AIDA-L, a layout generation tool, fully developed by the project team.

The AIDA-C tool implements an optimization-based sizing methodology based on a multi-objective multi-constrained optimization kernel, which uses an adapted version of the well-known NSGA-II optimization kernel developed by K. Deb. The synthesis process starts by a set of standard inputs, such as, a Spice-like netlist, a technology design kit from the target technology and a set of required performance specifications. Then, optimization process is executed generating a Pareto front of non-dominated optimal solutions for nominal working conditions, next, the optimization process passes to a more aggressive and challenging task which consists of including corners analysis into the optimization loop. During the optimization process industrial standard electrical simulators, such as, HSPICE®, ELSO® or Spectre® are considered as evaluation engines to guarantee extremely accurate results. Additionally, in order to increase the optimization process efficiency innovative modeling techniques were developed and implemented allowing a considerable reduction in terms of required simulations with benefits in terms of design time.

The AIDA-L tool implements an automatic layout generation methodology starting from a sized circuit schematic, a template description and the technology design kit. Then, the template is instantiated with sized analog modules, generated by a built-in and technology independent layout module generator (AMG), ending with the placement task. Next, the routing operation is performed following an innovative a multi-port multi-terminal analog routing approach, verified by built-in design rule checker (DRC), electric rule checker (ERC) and short circuit checker (SCC) modules leading to a final and complete error free GDSII layout description.

Finally, the practical usefulness of the proposed methodology was proved by designing several analog circuit building blocks of different levels of complexity, such as, operational amplifiers, LNAs, LC-VCOs, etc. for different integration technologies, e.g., UMC 130nm, XFAB 350nm, etc. Additionally, the proposed approach was implemented as a standalone application with interfaces with major CAD tools such as CADENCE IC Design Framework, so that, in can be easily embedded in the traditional AMS IC design flow, and so, be massively used by IC designers.

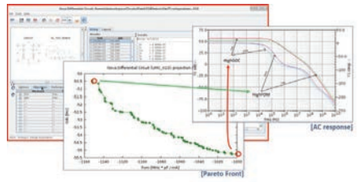

Fig.2 Pareto Optimal Front for the Circuit Level Sizing by AIDA-C.

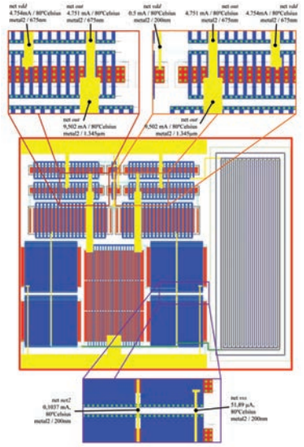

Fig.3 Fully Generated Two-Stage Amplifier Layout by AIDA-L.

ACHIEVEMENTS

The main project results are the AIDAsoft design environment prototype and two tools AIDA-C and AIDA-L developed along the project to address, respectively, the circuit level sizing and optimization and the layout generation, which are now in the fore front of the analog IC design automation state-of-the-art.

The international recognition of the work by the scientific community was achieved with several publications and 2 awards in international conferences, respectively, an Honorable Mention from SMACD 2012 Competition on Analog IC Design Automation and a Student Best Paper Award (Runner-Up) at IEEE ISCAS 2014..

The industry recognition of the AIDAsoft design environment value and the provided facilities to interface with state-of-the-art commercial analog design environments lead to a new cooperation with an international industrial player in the area of space technologies, namely, THALES Alenia Space in France.

INDICATORS	
FUNDING	42 K€
BOOKS	2
BOOK CHAPTERS	1
JOURNAL PAPERS	3
CONFERENCES PAPERS	8
MSC THESIS	2
PROTOTYPE	1

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PUBLICATIONS

- F. Rocha, R. Martins, N. Lourenço, N. Horta, "Electronic Design Automation of Analog ICs combining Gradient Models with Multi-Objective Evolutionary Algorithms" by Springer, SpringerBriefs, 2014 (ISBN: 978-3-319-02189-8).
- R. Martins, N. Lourenço, N. Horta, "Generating Analog IC Layout with LAYGEN II" by Springer, SpringerBriefs, 2013 (ISBN: 978-3-642-33145-9).
- N. Lourenço, R. Martins, M. Barros, N. Horta, "Analog Circuit Design based on Robust POFs using an Enhanced MOEA with SVM Models" - Chapter in Analog/RF and Mixed-Signal Circuit Systematic Design, Mourad Fakhfakh, Esteban Tlelo-Cuautle, Rafael Castro-Lopez, Springer, 2013.
- R. Martins, N. Lourenço, N. Horta, "LAYGEN II – Automatic Layout Generation of Analog Integrated Circuits", IEEE Transactions on Computer-Aided Design, vol. 32, no. 11, pp.1641-1654, 2013 (DOI: 10.1109/TCAD.2013.2269050).
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- R. Póvoa, N. Lourenço, N. Horta, R. Santos-Tavares, J. Goes, "Single-Stage Amplifiers with Gain Enhancement and Improved Energy-Efficiency employing Voltage-Combiners", Proc. IFIP/IEEE International Conference on Very Large Scale Integration (VLSI-SoC), Istanbul, Turkey, 2013.
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- N. Lourenço, N. Horta, "GENOM-POF: Multi-Objective Evolutionary Synthesis of Analog ICs with Corners Validation", Proc. ACM Genetic and Evolutionary Computation Conference (GECCO) , Philadelphia, USA, Jul. 2012.
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- Frederico Rocha, "Enhancing a Layout-Aware Synthesis Methodology for Analog ICs by Embedding Statistical Knowledge into the Evolutionary Optimization Kernel", MEEC, Instituto Superior Técnico – Technical University of Lisbon, concluded in Dec. 2012 with score 18 out of 20. (Co-Supervisor: Prof. João Paulo Carvalho – DEEC/IST)
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- AIDA Environment (www.aidasoft.com)

URL
http://www.it.pt/project_detail_p.asp?ID=1960