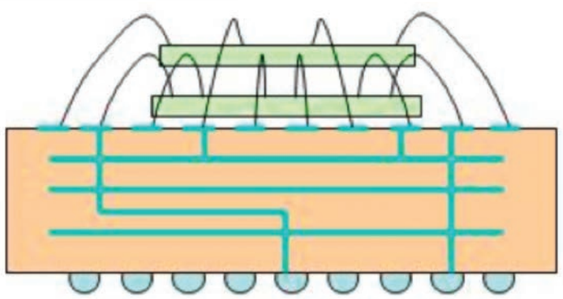
MOCHA

Modelling and Characterization for SiP Signal and Power Integrity Analysis

STREP-FP7 project dedicated to the analysis and development of technologies to improve Signal Integrity (SI) and Power Integrity (PI) analysis before the prototyping stage of System-In-Package integrated circuits. The IT-Aveiro participation consisted of the characterization and modeling of the output buffer stage of integrated circuits for generating SI/PI simulation models.



PROJECT WEBPAGE URL
http://www.it.pt/project_detail_p.asp?ID=964
http://www.mocha.polito.it/default.htm

Main Project Team

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Funding Agencies

European Community FP7	146k€
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Indicators

Journal Papers	2
Conference Papers	8
Concluded MSc	1

Two Main Publications

I. S. Stievano, L. Rigazio, F. G. Canavero, T. R. Cunha, J. C. Pedro, H. M. Teixeira, A. Girardi, R. Izzi, and F. Vitale, **"Behavioral modeling of IC memories from measured data",** IEEE Trans. on Instr. and Meas., vol. 60, no. 10, pp. 3471-3479, Oct. 2011.

TT. R. Cunha, H. M. Teixeira, J. C. Pedro, I. S. Stievano, L. Rigazio, F. G. Canavero, R. Izzi, F. Vitale, and A. Girardi, **"Validation by measurements of an IC modeling approach for SiP applications**", IEEE Trans. on Components, Packaging and Manufacturing Technology (former IEEE Trans. on Advanced Packaging), vol. 1, no. 8, pp. 1214-1225, Aug. 2011

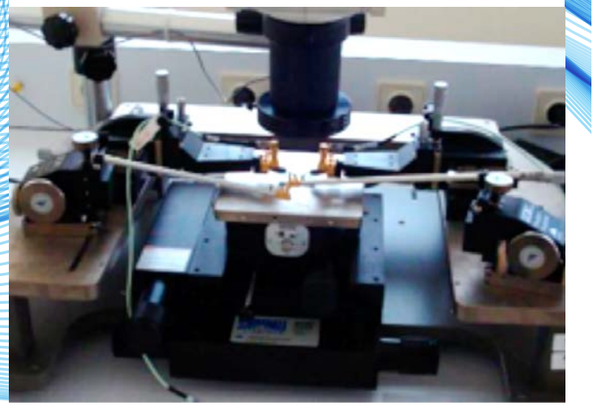

Fig. 1 Pre-processing part of the proposed low-complexity VDLL architecture

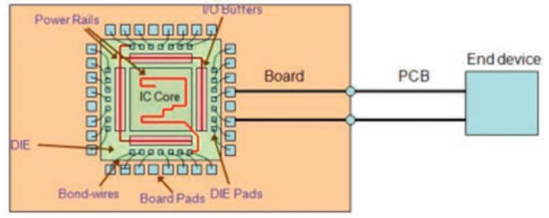

Fig. 2 Circular trajectory estimation with 500 samples, different cell sizes, and BPSK(1) modulation

Nowadays, modern electronic systems like mobile phones are integrating an increasing number of sophisticated and heterogeneous functions, such as GPS, video cameras and MP3 players. The key features of this revolution are the increase of system complexity, the development of new dense 3D packaging structures and the increase of signaling rates. The complexity, the large integration and the fast signals require the accurate prediction of the whole system performance in the early phase of the design. The aim of the MOCHA project was the development of a set of integrated EDA tools and modelling flows that combine the availability of accurate models for the new devices like advanced IC interfaces and RF components, either extracted by simulation or measurement, with a reliable system-level simulation for System-in-Package (SiP) design and verification.

The MOCHA project was organized into four major work packages (WP), which logically defined the different fields that have to be addressed in order to achieve the expected technical goals. The sequence the different global activities considered was: parametric macro-models' generation; 3D EM engine development; SI simulation and measurements strategies identification. At a final stage, these activities were merged together in the implementation of reliable simulation and measurement design verification platforms.

Besides the modelling of the IC nonlinear dynamic behaviour, the participation of the IT-Aveiro team was also focused on the identification of a suitable measurement methodology for modelling IC power supply distribution networks, overcoming the current limit of EDA tools to extract a reliable wide-frequency-range model. To this aim, both electromagnetic (EM) simulations and measurements were carried out, allowing to generate accurate models that can be effectively used to study the trade-off between power rails topology, buffers configuration, pads distribution and accuracy. The final model was targeted to be used for carrying out accurate power integrity simulations during the SiP design verification phase.

The developed modelling strategy is composed of three main interconnected sub-models. The first sub-model characterizes the nonlinear dynamic behaviour that the output stages (or output buffers) of IC devices present. The IC output buffers transmit the digital information (coded inside the IC through very low power signals) to the outer circuits to which the IC is connected. As output buffers are built of transistor stages, and since these ICs are aimed for high switching frequency operation, the nonlinear dynamic effects imposed by the output buffers are of decisive importance to the integrity of the coded information, thus it was mandatory to accurately model their behaviour.

A second sub-model of the considered approach consisted on the characterization of the behaviour of the IC power rails when operating under strong switching activity. The rail parasitics respond to current peaks by making the voltage supply bounce around the nominal value, which leads to undesired behaviour of the whole IC. Such behaviour must also be predicted in the design stage, demanding again for an accurate way of modelling this characteristic.

The third addressed sub-model was a simulation model for the IC core switching activity, estimating the current peaks that are demanded by the IC core when a high number of transistors are simultaneously switching.

The work of the IT-Aveiro team, together with the involved partners, led to the development of new modelling and IC device characterization strategies which were already incorporated into commercial circuit simulation platforms dedicated to IC circuit simulation. This is very important to allow IC developers to accurately test new circuits (namely, in the SiP configuration). In addition, two Ph.D. studies were started at IT-Aveiro under the topics of I/O buffer modelling and characterization; these works are now at their final stage.