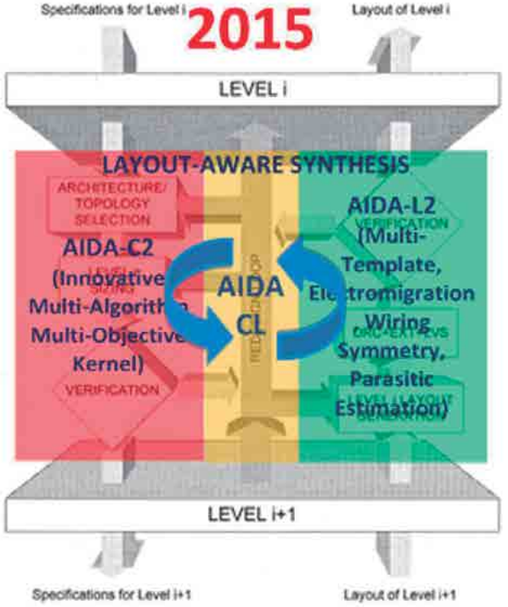
OPERA

Layout-Aware Analog IC Design Automation

The OPERA project addressed the definition, implementation and validation of an innovative layout-aware sizing and optimization approach (AIDA) applied to analog IC design. The proposed approach puts together the in-house EDA tools, AIDA-C, a circuit level sizing tool, and AIDA-L, a layout generator tool. The approach was validated for the design of state-of-the-art analog IC designs.



PROJECT WEBPAGE URL
www.aidasoft.com

Main Project Team

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Indicators

Funding	40k €
Books	3
Journal Papers	7
Conference Papers	17
Book Chapters:	2
Concluded PhD	2
Concluded MSc:	7

Two Main Publications

N. Lourenço, R. Martins, N. Horta, "Automatic Analog IC Sizing and Optimization Constrained with PVT Corners and Layout Effects", Springer, 2016 (ISBN: 978-3-319-42036-3).

R. Martins, N. Lourenço, N. Horta, "Analog Integrated Circuit Design Automation – Placement, Routing and Parasitic Extraction Techniques", Springer, 2016 (ISBN: 978-3-319-34059-3).

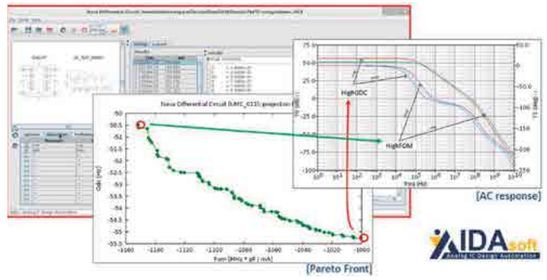

Fig. 1 AIDA-C Analog IC Multi-Objective Multi-Constraint Sizing, Optimization and Trade-off Exploration

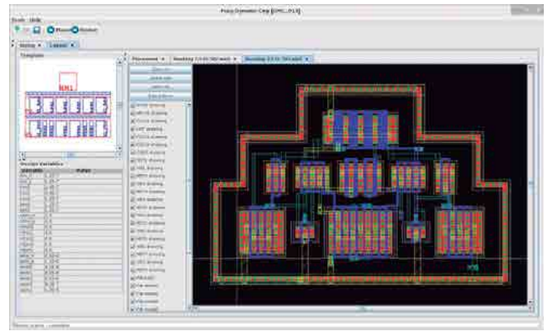

Fig. 2 AIDA-L Analog IC Layout Generation and Graphical User Interface.

GENERAL MOTIVATION AND OBJECTIVES

Most of the time, in analog integrated circuit design, is spent on sizing and optimization of devices. The non-linear relation between devices' sizes and circuits' performance is a complex problem, which is even harder when non-ideal layout effects are taken into account. Hence, due to the huge design space, it becomes extremely difficult for human designers to manage a good compromise between all specifications, and the design variables. Nowadays, there is no general and systematic way of producing new analog designs, even intellectual property reuse requires an expert designer to map designs into new technologies or new set of performance specifications. All the factors, previously mentioned, make analog design the bottleneck of AMS SoC designs. Furthermore, the degree of analog design automation is about 15% compared to digital and is expected to reach 50% by 2020, showing the growing interest of the design automation area, also due to the ever increasing number of AMS SoCs overall.

The main objective of the project is to attain a new electronic design automation (EDA) solution allowing the size and optimization of analog building blocks taking into account not only circuit level simulations but also layout effects leading to a state-of-the-art sizing and optimization methodology.

CHALLENGE

The challenge is to build an innovative EDA solution, which must incorporate both circuit level sizing and layout generation, with an accurate parasitic extractor allowing the back annotation of the circuit description and simultaneously an extremely efficient multi-objective multi-constraint optimization approach, to perform the global task in a reasonable design time and generating fully compatible output formats with the most used commercial IC design frameworks.

WORK DESCRIPTION AND ACHIEVEMENTS

The OPERA project proposes an innovative methodology for analog IC design automation. The existing AIDA-C and AIDA-L tools which compose AIDA, fully developed at ICG-LX, already implement the automatic sizing and layout generation but working as stand-alone tools. In order to boost the AIDA analog IC design automation environment, the OPERA project put together both AIDA-C and AIDA-L tools to reach a real and effective layout-aware synthesis process. This included, at circuit-level, the development of innovative solutions for the optimization kernel in order to cope with more complex synthesis process without compromising tool performance, and, at layout-level, the development of highly efficient and accurate placement and routing solutions. Therefore, in order to implement a layout-aware synthesis process and to reach the desired highly accurate solutions, AIDA-C considered three development tasks. The first task addressed the enhancement of the multi-objective multi-constrained optimization kernel, which was initially based on an adapted implementation of the NSGA-II algorithm, by developing and implementing innovative multi-objective optimization approaches. In the second task of development a floorplan-aware synthesis was implemented by estimating for each Pareto Optimal solution the most compact floorplan based on the instantiation of a diversified set of layout templates. In the third task the layout-aware synthesis was implemented by adding to the floorplan-aware approach the routing and layout parasitic estimation functionalities. Therefore, the AIDA-L tool was enhanced with additional developments, to reach a highly accurate layout-aware synthesis. Mainly, allowing multi-template exploration, enriching the in-house analog module generator to create and characterize additional transistor, capacitor, resistors and inductors layout structures, and boosting the routing module to handle electromigration, IR-drop, symmetry, etc.. Finally, the proposed approach was implemented as a standalone application with interfaces with major CAD tools such as CADENCE IC Design Framework, so that, in can be easily embedded in the traditional AMS IC design flow.